Synchronization Pulse Detection Circuit

Abstract of the Disclosure

A synchronization pulse detector for detecting a synchronization pulse within an input signal. The input

- 5 signal has "level" portions (i.e., substantially non-time varying portions) and "transition" portions (i.e., substantially time varying portions). The pulse detector includes a pulse shape detector for determining each time the input signal has a sequence of a first "level" portion,
- 10 followed by a first "transition" portion, followed by a second "level" portion, followed by a second "transition" portion followed by a third "level" portion, one of the first and second "transition" portions being positive and the other one of the first and second "transition" portions
- being negative. Each time such sequence is determined a pulse_shape detected pulse is produced. An evaluator is provided to reject invalid pulse_shape detected pulses. In one embodiment, the input signal is a video signal and the evaluator includes a time window for determining whether
- such shape_detected pulses are produced at a predetermined rate expected for the series of synchronization pulses. The evaluator includes a voltage window responsive to the produced shape_detected pulses and their associated values of the second "level" portions for determining whether one
- of such produced second "level" portions is substantially the same as or lower but not higher than the lowest DC value recorded during the time-equivalent of one line of video. The evaluator may include both the time window and the voltage window. The voltage window is mainly used to
- 30 acquire an initial lock to an unknown and not yet clamped video signal.